UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,713	04/16/2004	William D. Boyd	TI-37214	2185

23494 7590 05/22/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,713	BOYD ET AL.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**., 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *13-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-12 in the reply filed on 4/27/2006 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al (U.S. PG Pub #2002/0079592), in view of Egawa (U.S. Patent #6426554).

With respect to **claim 1**, Lo teaches providing a device unit (Fig. 8, 210), said unit having contact pads covered by a solderable metallic member (Fig. 8, 216); providing a wafer-level leadframe having a plurality of segment groups (Fig. 8, 202), each group suitable for one of said device units; connecting said wafer to said leadframe (Fig. 8, 218); encapsulating said assembled wafer and leadframe except for those segment portions intended for external connections (Fig. 8, 226); but does not teach providing the lead frame for a wafer having a plurality of device units, and singulating a encapsulated assembly of a wafer and a leadframe into discrete chip-size devices. Egawa teaches attaching a wiring layer (Fig. 1, 21) to a wafer (Fig. 1, 13), and then singulating the wafer and wiring

layer into discrete devices (Col 5 Ln 61-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the leadframe of Lo onto a wafer prior to singulating as taught by Egawa in order to efficiently produce the discrete device units.

With respect to **claim 4**, Lo teaches that the step of connecting is provided by means of solder paste (Col 3 Ln 50-52).

Claims 2, 3, 5, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo, in view of Egawa, further in view of Chow et al (U.S. Patent #6413851).

With respect to **claim 2**, Lo does not teach a copper stud. Chow teaches a copper stud (Col 4 Ln 47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a stud made of copper in the metal pad of Lo as taught by Chow in order to form a reliable electrical connection, as copper has a desirable conductivity.

With respect to **claim 3**, Lo does not teach a nickel stud. Chow teaches a nickel stud (Col 4 Ln 60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a stud made of nickel in the metal pad of Lo as taught by Chow in order to form a reliable electrical connection, as nickel has a desirable conductivity.

With respect to **claim 5**, Lo teaches providing a device unit (Fig. 8, 210), said unit having an active surface (Fig. 8, 212), a plurality of patterned metal

contact pads (Fig. 8, 216), each contact pad having an outer surface suitable to form metallurgical bonds without melting (Col 3 Ln 50-52); providing a leadframe suitable for the device unit (Fig. 8, 202), each segment having first and second ends covered by solderable metal (Fig. 8, inner and outer ends of leads 202, respectively); placing a predetermined amount of solder paste on each of said first segment ends (Col 3 Ln 50-52); aligning said leadframe with said wafer so that each of said paste-covered segment ends is aligned with the corresponding metal stud of the respective device unit (Fig. 8, 218); connecting said leadframe to said wafer by contacting said metal studs and said first segment ends and reflowing said solder paste (Col 3 Ln 50-52); encapsulating said wafer in a molding compound so that said device units and said first segment ends are covered, while said second segment ends remain exposed (Fig. 8, 226); but does not teach that a leadframe having a plurality of segment groups for each device unit is placed on a wafer having a plurality of device units, or separating an encapsulated wafer and leadframe into individual encapsulated device units to create a plurality of assembled, package semiconductor devices. Egawa teaches attaching a continuous conductive film having a wiring pattern (Fig. 2, 21) for each device unit (Fig. 1, 13) to a wafer (Fig. 1, collective of many devices 13), and then singulating the wafer and wiring layer into discrete devices (Col 5 Ln 61-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the leadframe of Lo, having a segment

group for each device unit, onto a wafer prior to singulating as taught by Egawa in order to efficiently produce the discrete device units.

Furthermore, Lo does not teach that the device unit is protected by an overcoat, said overcoat having a plurality of windows exposing the metal contact pads, a patterned barrier metal layer on said pad metal in said windows and on portions of said overcoat, which surround the perimeter of said windows, or a plurality of patterned metal studs, one stud each on a barrier layer. Chow teaches a chip having an overcoat (Fig. 1, 6) having a plurality of windows exposing a metal contact pad (Fig. 1, 4); a barrier metal layer on said pad and on portions of said overcoat (Fig. 1, 8); and a plurality of patterned metal studs one stud each on a barrier layer (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an overcoat, barrier metal, and metal studs on the chip of Lo as taught by Chow in order to create a reliable electrical connection.

With respect to **claim 6**, Lo does not teach the step of separating said encapsulated wafer comprises a sawing technique. Egawa teaches sawing a wafer to form separate devices. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form multiple device on the same wafer and saw the wafer as taught by Lo in order to efficiently produce multiple discrete devices.

With respect to **claim 8**, Lo teaches that said device units are integrated circuits (Col 1 Ln 13).

With respect to **claim 9**, Lo teaches that said assembled, packaged semiconductor device are chip-scale devices (Col 1 Ln 21).

With respect to **claim 10**, Lo teaches that prior to the step of encapsulating, the step of attaching a metal sheet to the wafer surface opposite to said active device surface so that the sheet surface opposite said attached surface remains exposed after said step of encapsulating (Fig. 7, 230).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo, in view of Chow.

With respect to **claim 11**, Lo teaches providing a device unit (Fig. 8, 210), said unit having an active surface (Fig. 8, 212), a plurality of patterned metal contact pads (Fig. 8, 216), each contact pad having an outer surface suitable to form metallurgical bonds without melting (Col 3 Ln 50-52); providing a leadframe suitable for the device unit (Fig. 8, 202), each segment having first and second ends covered by solderable metal (Fig. 8, inner and outer ends of leads 202, respectively); placing a predetermined amount of solder paste on each of said first segment ends (Col 3 Ln 50-52); aligning said leadframe with said wafer so that each of said paste-covered segment ends is aligned with the corresponding metal stud of the respective device unit (Fig. 8, 218); connecting said leadframe to said wafer by contacting said metal studs and said first segment ends and reflowing said solder paste (Col 3 Ln 50-52); encapsulating said wafer in a molding compound so that said device units and said first segment ends are

covered, while said second segment ends remain exposed (Fig. 8, 226); but does not teach that the device unit is protected by an overcoat, said overcoat having a plurality of windows exposing the metal contact pads, a patterned barrier metal layer on said pad metal in said windows and on portions of said overcoat, which surround the perimeter of said windows, or a plurality of patterned metal studs, one stud each on a barrier layer. Chow teaches a chip having an overcoat (Fig. 1, 6) having a plurality of windows exposing a metal contact pad (Fig. 1, 4); a barrier metal layer on said pad and on portions of said overcoat (Fig. 1, 8); and a plurality of patterned metal studs one stud each on a barrier layer (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an overcoat, barrier metal, and metal studs on the chip of Lo as taught by Chow in order to create a reliable electrical connection.

With respect to **claim 12**, Lo teaches the step of attaching a heat spreader surface to the chip surface opposite said active surface prior to said step of encapsulating so that the spreader surface opposite said attached surface remains exposed (Fig. 7, 230).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo, Egawa, and Chow, in view of Huang (U.S. Patent #6384472).

With respect to **claim 7**, Lo and Egawa do not teach that the step of separating said encapsulated wafer comprises a laser cutting technique (Col 5

Ln 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a laser to separate the encapsulated wafer of Lo and Egawa in order to cut along a scribe line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EVAN PERT
PRIMARY EXAMINER

bps